VertexCom

VC7300-Series Product Brief

Version: 1.1

Release Date: June 20, 2019

General Description

The VC7300-series is a highly integrated wireless MCU which is a perfect fit to IoT networking and sensing applications. It integrates Cortex-M3 MCU, 512/1024 KB Flash, 128 KB SRAM, sub-GHz radio and other functionalities such as UART/SPI/I^{2}C, WDT and Timer, etc. The VC7300-series has varieties of power saving modes which can be leveraged to build ultra-low power IoT networks with powerful computing capability. The embedded sub-GHz RF transceiver features low power consumption, long-range and robust wireless links, being able to reject large nearby interfering RF signals.

Key Features

- ARM Cortex M3 CPU core with 512/1024 kB flash and 128 kB RAM
- Best-in-class RF performance with VC7000 sub-GHz RF transceiver
- AES accelerator of 128/192/256-bit keys
- Ultra-low power wireless SoC
  - RX mode: 18 mA
  - TX mode:
    - 45 mA@+13 dBm
    - 110 mA@+20 dBm
  - Sleep mode:
    - VC7300A: 2.5 uA
    - VC7300B: 9 uA~10 uA
  - Deep sleep mode: 1.1 uA
- AES accelerator of 128/192/256-bit keys

MCU Features

- MCU
  - 32-bit Cortex M3 with maximum 39.3126 MHz operation speed
  - Single cycle multiplier
  - Standard 2-wires SWD debug interface
  - 512 KB Flash with write protect, support both IAP and ISP
  - 128 KB SRAM with parity check and data retention under sleep mode
  - 16 KB SRAM with data retention under deep-sleep mode
  - Support abort exception detection including Flash check-sum error, SRAM parity error, memory address error and memory align error

- Support boot from embedded flash or boot from internal ROM with IO strap option

- Interface Controller
  - Support SPI flash and SPI SRAM for program execution and directly data read/write
  - 4 UART controllers with parity check and transmit/receive FIFOs
  - Each IR channel can be coupled with IR carrier for IR transmission
  - 1 SPI master/slave controllers
  - 1 I^2C master/slave controller
  - 4 32-bit timers
  - 4 16-bit PWM timers
  - 4-channel DMA controller
  - 128/192/256-bit AES CODEC
  - ECC encrypt/decrypt accelerated engine
  - Watch dog timers with programmable period
  - Support multiple wake-up sources under each mode
  - Maximum 35 GPIOs
  - 11 GPIOs can be external interrupt and wakeup sources under all modes
  - Support key scan controller which can support up to 16 keys with 4x4 matrix

- Analog Controller
  - 10-bit ADC with 1 Msps and 6 external inputs
  - ADC supports manual sample mode or auto sample mode
  - 1 comparator with single end input or differential input
  - Embedded 32 KHz and 39.2166 MHz RCO
  - Support external 32 KHz crystal
  - Support crystal absent detect for 32 KHz
  - Each clock can be selected to be system clock
  - Support digital clock divider up-to 1/256
  - Support low voltage detection with programmable level
  - Support power-on reset for both IO voltage and core voltage
  - Support 1ppm RTC auto-calibration under deep-sleep mode
  - Support true random number generator (TRNG) and pseudo random number generator

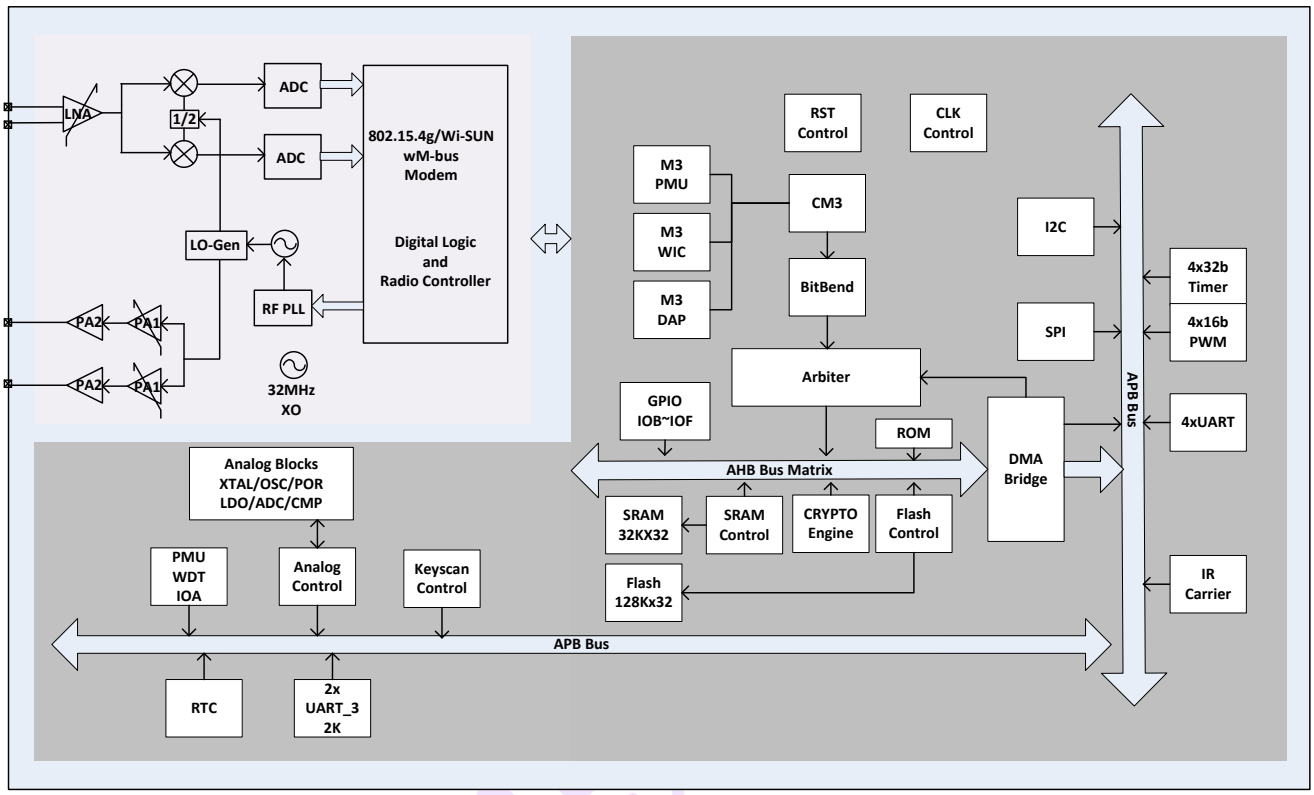
Radio Features (VC7000)

- Support IEEE 802.15.4g/Wi-SUN
- Support wireless M-Bus
- ISM frequency bands: 315, 433, 490, 868, 915 MHz
- Excellent selectivity performance
  - Adjacent channel rejection: 48 dB
  - Blocking performance: 75 dB
- Best in class receiver sensitivity
  - -109 dBm at 50 kbps GFSK
- Maximum data rate: 300 kbps
- Configurable maximum transmit output power
  - +20 dBm
  - +13 dBm
- Automatic output power ramping
- Modulation schemes: OOK, (G)FSK, 4(G)FSK and GMSK
- Automatic RX wake-up for low power listen
- Fast wake-up and AGC for low-power listen
- Functions for communication robustness
  - RF channel hopping
  - Retransmission
  - Auto-acknowledgement
- Digital RSSI and clear channel assessment for CSMA and listen-before-talk systems
- Support packet over packet reception for reliable communication
- Early termination of receive mode for incorrect preamble reception
- Hardware-based user identification listen to eliminate false wake-up

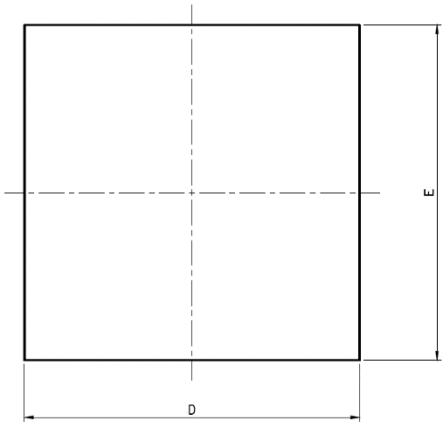
System Features

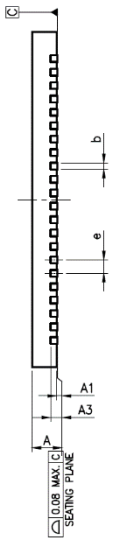
- Operating Voltage: 2.0 V ~ 3.6 V
- Package: QFN-64 (9 x 9mm)
- Operation Temperature: -40~+85 °C

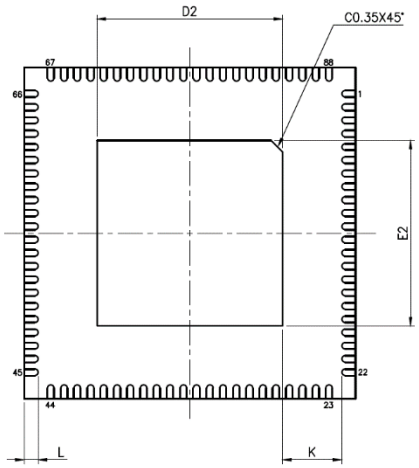
Block Diagram



Package Information







	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(XA88)			VQFN(YA88)		
SYMBOLS	MIN.	NOM.		MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
D	10.00 BSC			10.00 BSC		
E	10.00 BSC			10.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			b			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
276X27* MIL	6.75	6.80	6.85	6.75	6.80	6.85	0.15	0.20	0.25	V	X	(W)VNNE-1

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Ordering Information

Part No.	Description	Frequency Band	Standards	MCU	Flash	RAM	PKG	Body Size
VC7300AU	Sub-GHz Wireless MCU	315, 433, 490, 868, 915 MHz	IEEE 802.15.4g, Wi-SUN, Wireless M-Bus	ARM Cortex M3	512 KB	128 KB	QFN-64	9 x 9mm
VC7300BU	Sub-GHz Wireless MCU	315, 433, 490, 868, 915 MHz	IEEE 802.15.4g, Wi-SUN, Wireless M-Bus	ARM Cortex M3	1 MB	128 KB	QFN-64	9 x 9mm